Power and performance optimization through MPI supported dynamic voltage and frequency scaling

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Abstract

The Intel Single Chip Cloud Computer (SCC) architecture offers the adjustment of voltage and frequency on individual islands in a certain range and in a certain dependency to each other. This possibility offers a high degree of freedom for workload balancing which can be done statically (at compile time) or dynamically (at run-time). Especially the latter topic, the dynamic voltage and frequency scaling (DVFS) is of high interest for novel multiprocessor systems, if they are deployed in energy efficient systems. It enables to provide computing performance on demand and therefore reduces power consumption. We envision to develop models, methods and cost functions for the DVFS in order to optimize the workload balance of all processor cores at run-time on the SCC.

Keywords: DVFS, Dynamic MPI, workload balancing

1. Introduction

The Intel Single Chip Cloud Computer (SCC) architecture offers the adjustment of voltage and frequency on individual islands (consisting of 24 frequency and 7 voltage domains) in a certain range and in certain dependency to each other. This possibility offers a high degree of freedom for workload balancing which can be done statically (at compile time) or dynamically (at run-time). Especially the latter topic, the dynamic voltage and frequency scaling (DVFS) is of high interest for novel multiprocessor systems, if they are deployed in energy efficient systems. It enables to provide computing performance on demand and therefore reduces power consumption. We envision to develop models, methods and cost functions for DVFS in order to optimize the workload balance of all processor cores at run-time on the SCC. For this purpose, novel modules for MPI will be developed in order to support the programmer through an autonomous performance / power consumption management. Furthermore, the modules which include the methods and cost functions for the DVFS avoid critical constellations of voltage and frequency which might lead to damage on the SCC. The challenging research topic delivers an extension to the MPI-based programming model through the support of DVFS on the SCC and closes therefore a gap for a novel MPSoC programming methodology. As a result, a reduced power consumption and simultaneously optimized performance increases the attractiveness of the SCC in a variety of application scenario and might open new markets for this and future multiprocessor systems. Especially the embedded high performance applications such as image processing for surveillance of rooms e.g. in an airport, benefit from a dynamic control of the MPSoC architecture in order to optimize power consumption tailored to a current situation. The research, which is proposed, follows the trend of cyber-physical systems, where a close control loop is used to optimize the system characteristic (see [1]). The benefit of the novel method will be measured under real conditions (a realistic application scenario) and compared to the traditional realization. All hardware related methods lead to a novel paradigm called Dynamic MPI. The SCC architecture with its MPI (Message Passing Interface) API is an excellent platform for studying and evaluating new programming paradigms. The research objective of this proposal is to define and implement a novel programming standard together with a designflow for efficiently programming heterogeneous and homogeneous multiprocessor systems. The idea is to extend the existing MPI standard with dynamic aspects. Out of this results the new programming paradigm: Dynamic MPI.

2. Relationship to other research at KIT and IOSB and previous work

The ITIV is working successfully on run-time adaptive systems over 9 years. In the area of reconfigurable hardware the group counts to the leading researchers in the world. The ITIV was responsible for the realization of the network-on-chip, the on-chip integration of the reconfigurable tiles and the run-time system support for the MORPHEUS chip (see [2]). Within this project, funded by the EU, the novel concepts of dynamic workload balancing were investigated successfully for this multicore chip. The proposed research with the SCC differs from the previous work besides MORPHEUS, several DFG funded projects and bilateral research projects in that way, that a fully new concept of a homogeneous processor array which follows the
programming model MPI can be used to optimize the performance and power consumption of the MPSoC. The project enables to gain the experience in run-time adaptive systems and enable to develop a standard programming model through an extension of MPI which is then available for the community.

To the best of our knowledge there exists so far no similar research on Dynamic MPI and its designflow as proposed here. The most similar approach is our own designflow (see [3]) from RAMPSoC, which supports the MPI-standard. RAMPSoC is a heterogeneous FPGA-based MPSoC consisting of a variable number of processors closely coupled with hardware accelerators. RAMPSoC exploits dynamic and partial reconfiguration to adapt the hardware structure of the MPSoC at runtime. For the runtime management of RAMPSoC a special purpose operating system called CAP-OS was developed. The designflow so far does not handle the dynamic aspects, which are planned for the here proposed Dynamic MPI. The research strengths at IOSB are the development of the architecture, the designflow and the runtime management system for heterogeneous multiprocessors based on FPGAs. Furthermore, a great research strength of our institute is the development of image processing algorithms, especially as the above mentioned object detection and tracking algorithms.

3. Impact of the research

The result of this research is an extension of the MPI programming model for the SCC chip. It is envisioned to gain the attractiveness of the SCC for a wide area of applications. Since power and performance can be optimized simultaneously through DVFS, but this design space is huge and practically not to handle by the designer, the programming model, the modules and the autonomous methods enable to handle this powerful feature of the new SCC chip. It is envisioned to reduce the power consumption by up to 50% in comparison to an application which is realized with traditional MPI. The application will be selected out of a scenario for image processing in embedded systems (a focus is here homeland security with surveillance cameras). The results will be delivered as an extension for MPI and distributed to the community together with Intel. Furthermore, the output of the research gives a feedback to Intel in terms of the requirements for DVFS. This means that the requirements of the granularity for the adjustment of voltage and frequency were evaluated. A result could be that less stages for the adjustment are sufficient for optimizing the system characteristic which leads to an decrease of chip area and therefore reduced costs. Furthermore, it is planned to extend and create a new programming standard for homogeneous as well as heterogeneous MPSoCs called Dynamic MPI together with a corresponding designflow. With these results, we want to provide a first solution for efficiently programming the SCC architecture and also existing and future architectures consisting of heterogeneous or homogeneous processing elements. Especially, we focus on the modeling of dynamic aspects, e.g. workload balancing depending on inputs from the environment within our programming paradigm. So far, to the best of our knowledge, these dynamic aspects are not handled by any programming paradigm. The envisioned extension of MPI enables to exploit the benefit of a dynamic allocation of processes on an MPSoC through standardized methods included in the MPI library.

4. Preliminary results

In order to explore the performance and power consumption tradeoff of the SCC two image processing applications have been selected and programmed using RCKMPI. The overall execution time and power consumption have been measured by varying the number of processing elements and their clock frequency.

4.1. Image processing applications

The first image processing algorithm is the sobel operator. This is an edge detection algorithm, which calculates the gradient magnitude at each point in a grey level image. It is often used to separate between objects and their background. The operator works with two convolution masks, one for horizontal changes and one for vertical ones. These masks slide over the image and compute the two derivative images. However, the sobel operator is a direction-independent edge detector, so the two results are normed (by the Pythagoras Theorem) and a direction-independent image is created. The characteristics of the sobel algorithm are many multiplications, additions and also square root operations.

The second image processing algorithm is a thinning algorithm. These algorithms are used to reduce two-dimensional objects to single pixel wide branches by removing pixels inside the object shape according to some criteria, but they do not shorten or break the object shape apart. Here a thinning algorithm, developed by Z. Guo and W. R. Hall [6], is used. This algorithm uses two subiterations, the first subiteration deletes the north and east and the second deletes the south and west outline points of the shape. For more information about this algorithm see [6] and [7]. The characteristics of this algorithm are multiple compare and jump operations.

Figure 1 shows the input image used for the exploration and the result images of the Sobel and the thinning algorithm.
Figure 2 shows the number of required clock cycles for the Sobel algorithm. With the increase of the number of cores it can be seen, that the effect of clock cycle reduction comes to saturation. A number of 24 cores is for this implementation of the Sobel algorithm the best choice. Certainly, algorithm and communication optimization can lead to slightly other results.

A other effect can be found with the thinning algorithm where a nearly linear speedup can be found. Therefore the maximum number of cores used to perform this application is of high benefit.

5. Conclusions and outlook

Currently the workgroups work in parallel on hardware related topics like the scaling of the voltage and frequency scaling mechanisms and the extension of the MPI standard as well as required virtualization techniques (see [4]). Here MPI methods for an FPGA-based MPSoC are presented. The groups intend to extract from this work the experience for the SCC related MPI extensions. Furthermore, attractive application scenarios from image processing, bioinformatics as well as from simulation acceleration are the use cases (see [5]).

Next steps of this research work is to include the realized MPI extensions and the control loops for the physical adjustment of voltage and frequency in more application scenarios in order to measure the impact and derive important parameter sets for the control loop equations. Currently an interdisciplinary discussion with experts from control engineering leads to a promising very novel technical experience which can lead to a fully new control mechanism for the SCC and SCC like architectures.
6. References


